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High-Quality Solution-Processed Silicon Oxide Gate Dielectric Applied on Indium Oxide Based Thin-Film Transistors

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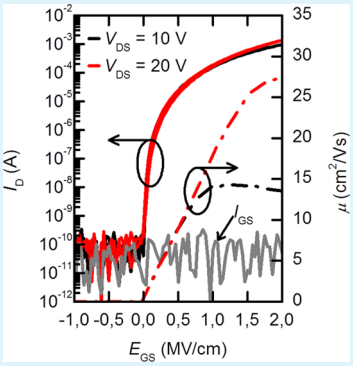
Supporting Information

ABSTRACT: A silicon oxide gate dielectric was synthesized by a facile sol–gel reaction and applied to solution-processed indium oxide based thin-film transistors (TFTs). The SiO_x sol–gel was spin-coated on highly doped silicon substrates and converted to a dense dielectric film with a smooth surface at a maximum processing temperature of T = 350 °C. The synthesis was systematically improved, so that the solution-processed silicon oxide finally achieved comparable break downfield strength (7 MV/cm) and leakage current densities (<10 nA/cm^2 at 1 MV/cm) to thermally grown silicon dioxide (SiO_2). The good quality of the dielectric layer was successfully proven in bottom-gate, bottom-contact metal oxide TFTs and compared to reference TFTs with thermally grown SiO_2. Both transistor types have field-effect mobility values as high as 28 cm^2/(Vs) with an on/off current ratio of 10^8, subthreshold swings of 0.30 and 0.37 V/dec, respectively, and a threshold voltage close to zero. The good device performance could be attributed to the smooth dielectric/semiconductor interface and low interface trap density. Thus, the sol–gel-derived SiO_2 is a promising candidate for a high-quality dielectric layer on many substrates and high-performance large-area applications.



KEYWORDS: *sol–gel, silicon oxide, solution-processed, thin-film transistor, indium oxide, high mobility*

INTRODUCTION

Since the early 1990s, a new rapidly developing economy has come into the focus of research and development: macroelectronics.[1,2] Unfortunately, up to now, current liquid-crystal displays (LCDs) are manufactured by cost-intensive vacuum processes like sputtering and chemical vapor deposition techniques,[3] which include some limitations in mass production and in realization in large-area electronics. For this reason, intensive research has been done in the development of solution-processed metal oxide films because of its simplicity, low cost, and high performance. These films are promising candidates to replace amorphous silicon as the active layer used in thin-film transistors (TFTs) as a switching device, e.g., for display applications and optoelectronic devices.[4−7] Indium oxide based TFTs provide high mobility, which is necessary for advanced display technologies such as 8K ultrahigh-definition, large-size televisions and organic light-emitting diode (OLED) displays.[6,8]

While solution-processed metal oxide semiconductors have made enormous progress in the past few years,[9−11] there is less research activity toward the development of solution-based novel dielectrics; only a few comprise both.[3,12−14] Most reports on solution-processed semiconductors were made on thermally grown silicon dioxide (SiO_2) or vacuum-deposited dielectrics.[15−18] To deposit the gate dielectric from a liquid phase, sol–gel chemistry offers a simple method to synthesize solutions for dielectric films and to tune the properties of the resulting product.[8] In many studies concerning solution-processed gate dielectrics, several deposition steps are necessary to achieve a desirable film thickness and low leakage currents.[3,19,20] This increases the process complexity and manufacturing costs. Here, we use just one deposition step to achieve desirable dielectric properties like high electric breakdown field strength, low leakage current, and low interface trap density, which is essential for high-performance electronics.[21] Comparable studies on solution-processed silicon oxide achieved leakage current densities that were 2 orders of magnitude higher[22,23] or required considerably higher annealing temperatures (T > 450 °C) to achieve similar results.[11] This is not suitable for high-performance (flexible) electronic devices. Although the synthesis route of the sol–gel-derived silicon oxide in this paper is similar to that presented in the paper of Cavas et al., the properties (dielectric constant, refractive index, and surface roughness) presented by Cavas et al. are far away from those of thermally grown SiO_2.[24] A study concerning the influence and role of the material composition and processing parameters of the sol–gel has been completely missing until now.

In this study, we synthesized a solution-processed silicon oxide by a facile sol–gel reaction. The dielectric properties nearly achieved the results obtained from thermally grown SiO_2. By optimizing the synthesis and processing technique, we achieved leakage current densities of less than 1×10^{-8} A/cm^2 at an applied electric field of 1 MV/cm with a maximum

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annealing temperature of 350 °C. To investigate the quality of the insulator in an electronic device, we combined this solution-processed SiO_2 with the solution-processed indium oxide based semiconductor iXsenic S (provided by Evonik Industries AG) to prepare high-performance TFTs.[25−29] The devices exhibit a mobility of 28 $cm^2/(Vs)$, an on/off ratio above 10^8, no hysteresis, and a subthreshold swing of about 0.30 V/dec.

EXPERIMENTAL SECTION

The sol−gel solution was synthesized by dissolving 0.52 g of tetraethyl orthosilicate (TEOS; Sigma-Aldrich, 99.999% trace metals basis) in 1.0 g of isopropyl alcohol (IPA; Sigma-Aldrich, anhydrous 99.5%), 0.1 g of deionized water, and 0.1 g of 0.1 M nitric acid (Sigma-Aldrich). The whole solution was stirred at room temperature for 5 min. After that, the solution was diluted with 1.28 g of IPA and stirred again for 2 min. Finally, the solution aged for about 6.5 h at room temperature before it was spin-coated on highly p^+-doped silicon substrates. The dielectric properties were characterized in a metal−insulator-semiconductor (MIS) structure. Therefore, the substrates were cleaned in a standard cleaning process with acetone and IPA. Additionally, the substrates were placed for 10 min in an ozone cleaner to remove organic residuals from the surface and to improve the wettability. Subsequently, 100 μL of the sol−gel solution was dropped onto the substrate and spin-coated at 2000 rpm for 30 s. Conversion of the sol−gel to a dense silicon oxide film was done stepwise: First of all, the substrates were placed on a hot plate at 120 °C for 10 min to slowly evaporate the containing water and the solvent. Next, the film was cross-linked under UV light for 10 min in the ozone cleaner and then annealed on a hot plate at 210 °C for 10 min. The final curing was done for 30 min at 350 °C. For the metal contacts, 80 nm of aluminum were thermally evaporated through a shadow mask in an EB3 thermal evaporator from BOC Edwards Ltd. The contact area of the resulting pads was 1.2 mm^2.

The bottom-gate, bottom-contact TFTs were processed on an n^+ silicon substrate acting as the bottom-gate electrode. The solution-processed silicon oxide was prepared as described above. For the reference devices, the 230 nm SiO_2 was thermally grown. The indium−tin oxide/gold (ITO/Au) electrodes were prepared on the gate dielectric by UV lithography, sputtering (ITO), electron-beam evaporation (Au), and a lift-off technique. Therefore, a positive photoresist (AZ1514H, Micro Chemicals) was deposited by spin-coating and exposed to UV light (λ = 365 nm) through a photomask in a MJB 3 mask aligner from SUSS Micro Tec. The photoresist was developed using the AZ Developer from Micro Chemicals. The samples were pretreated in the ozone cleaner for 10 min. The solid indium-based metal oxo−alkoxide precursor (iXsenic S, Evonik Industries AG) was spin-coated under atmospheric conditions at 4000 rpm for 30 s and annealed at 350 °C for 1 h. Outside of the active channel region, the metal oxide film was removed by conventional UV lithography and wet etching in oxalic acid (c = 1 mol/L). The acid was heated to T = 50 °C to decrease the etching time to 10 min. The channel width to channel length ratio (W/L) was 200/20.

The layer thickness and refractive index of the oxide film were estimated from ellipsometry using a Sentech Sen-pro ellipsometer. The extracted layer thickness was compared with values taken from atomic force microscopy (AFM; Nanosurf, Mobile S). The depth of a groove in the solution-processed silicon oxide was measured to obtain the layer thickness. Microscope and scanning electron microscopy (SEM) micrographs were taken using a Leica DM 2500 M optical microscope and a Phenom scanning electron microscope from PEI, respectively. To extract the permittivity of the dielectric material, capacitance−voltage ($C-V$) measurements were done using an Agilent E4980 A LCR meter. For the current−voltage ($I-V$) characteristics of the TFTs and MIS structures, a semiconductor parameter analyzer (Agilent 4156B) was used. The fabricated TFTs were characterized under a nitrogen atmosphere at T = 300 K to avoid any influence from the ambient environment on the transistor performance.

RESULTS AND DISCUSSION

First of all, the film thickness and topography were investigated depending on the TEOS precursor concentration in the solution. The ratio between water and the TEOS precursor was kept constant to control the hydrolysis reaction. In order to decrease the total TEOS concentration, the solution was diluted with IPA. Film cracking is a problem, while the sol−gel coating is dried. Tensile stress during the drying and thermal treatment can lead to cracks if the film thickness exceeds a critical thickness.[30] Figure 1 shows optical micrographs of SiO_x

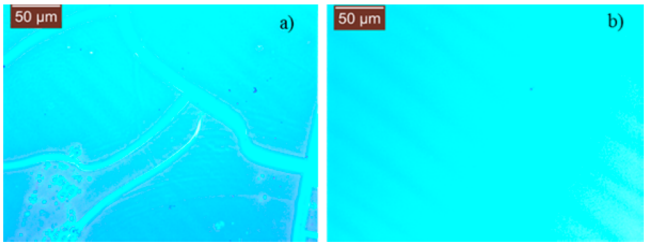

Figure 1. Optical micrographs of solution-processed SiO_x layers. The TEOS concentration within the solution amounts (a) c = 0.9 mol/L and (b) c = 0.8 mol/L, respectively.

films, which were prepared from solutions containing a TEOS concentration of 0.9 mol/L (Figure 1a) and 0.8 mol/L (Figure 1b), respectively. Figure 1a shows cracks in the dielectric layer after annealing, which primarily occur at the edges of the substrate. At the edges, the film thickness is increased, leading to a larger number of cracks. With decreasing film thickness (i.e., lower TEOS concentration), the films turn into defect-free films (Figure 1b). Thus, the maximum concentration of TEOS in the solution was determined as c = 0.8 mol/L to avoid the creation of cracks in the film.

Figure 2a shows the resulting film thickness of the insulator after processing with respect to the TEOS concentration. The

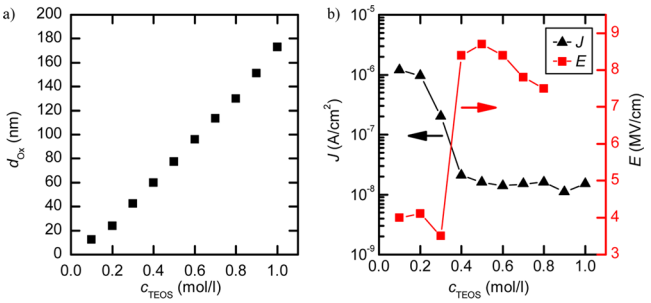

Figure 2. (a) Film thickness of the SiO_x layers with respect to the TEOS concentration. (b) Leakage current density measured at 1 MV/cm and a breakdown field strength for SiO_x layers with different TEOS precursor concentrations.

film thickness decreases (Figure 2b) from 180 nm (c = 1 mol/L) to 10 nm (c = 0.1 mol/L). Dielectric films prepared from a solution with a TEOS concentration higher than 0.3 mol/L exhibit a leakage current density of about 2×10^{-8} A/cm^2 (Figure 2b) and a breakdown field strength above 7 MV/cm (no breakdown was observed for concentrations above 0.8 mol/L). The leakage current density was extracted at an applied electric field of 1 MV/cm.

With decreasing TEOS concentration, the leakage current density increases to values larger than 1×10^{-6} A/cm^2 and the

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breakdown field strength drops to values of about 3−4 MV/cm. A topographical characterization of the films with AFM and SEM gives us a better understanding of this phenomenon. The films processed from solutions containing a precursor concentration of less than 0.3 mol/L show large holes in the dielectric layers (Figure 3).

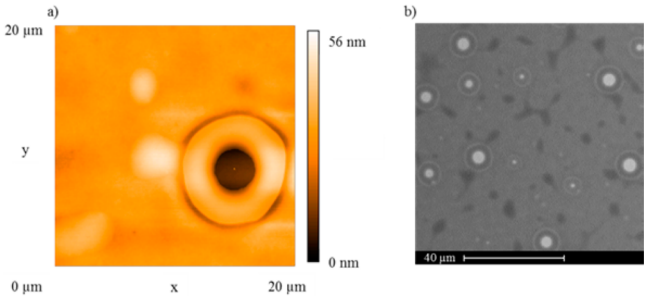

Figure 3. (a) Top-view AFM micrograph and (b) SEM micrograph of a SiO_x surface derived from a TEOS−sol solution containing a TEOS precursor concentration of 0.3 mol/L.

These holes have a diameter of around 5 μm a typical depth of 50 nm, and we find around one or two of these holes in an area of 20 μm × 20 μm. The value of 50 nm corresponds to the total thickness of the dielectric layer derived from a sol−gel solution containing a TEOS concentration of 0.3 mol/L. We assume that these holes are generated by evaporation of the solvent during the annealing process. Around the holes, the thickness of the dielectric layer is much lower, and hot spots of the applied electric field are created during the electrical measurement. This explains the increase of the leakage current density and the reduced breakdown field strength. Holes are also observed for films prepared from solutions with higher TEOS concentrations, but the diameter and depth of the holes are reduced, which explains the improved dielectric properties. Here the holes have a typical diameter of 100 nm and a depth of about 8 nm, which is much smaller than the total thickness ($d \gg 60$ nm). We find around 10 holes in an area of 2 μm × 2 μm. The surface roughness of the solution-processed SiO_x in areas where no holes are located amounts to 0.6 nm and is comparable to the surface roughness of thermally grown SiO_2 (R_q = 0.5 nm). These preliminary examinations show that for application as a gate dielectric in electronic devices the film thickness of the solution-processed SiO_x should be between 60 and 150 nm.

An important key parameter in the sol−gel chemistry is the pH value of the solution. It has a strong influence on the condensation and hydrolysis rates as well as on the structural properties of the final product.[31] In this study, we chose an acid-catalyzed sol−gel process. The pH value was controlled by the molarity of nitric acid. To get better insight into the chemistry, different silicia xerogels were prepared with different molarities of nitric acid ranging between 0.01 and 4.0 mol/L. The TEOS concentration (c = 0.8 mol/L), as well as the TEOS-to-H_2O ratio, was kept constant. The gelation time for all solutions was 7 h. Before the spin-coating process, the solutions were filtered through a 0.2 μm poly(tetrafluorethylene) syringe filter. For the lowest molarity of the appointed nitric acid (0.01 mol/L), no film formation on the silicon substrates was observable after the spin-coating and annealing process. The acid acts as a catalyst for the sol−gel reaction, which is a combination of hydrolysis and condensation reactions. The aging time of 7 h is too short for the low molarity of nitric acid to form Si−O−Si bonds by hydrolysis and condensation. For higher acidities, SiO_x colloids or network structures have already grown so that dielectric films are formed on the substrates. The thickness of the films varies between 142 nm (c_{HNO_3} = 0.1 mol/L) and 152 nm (c_{HNO_3} = 4.0 mol/L). The leakage current density and refractive index were investigated with respect to the molarity of the acid. Figure 4a shows an increase of the leakage current density with

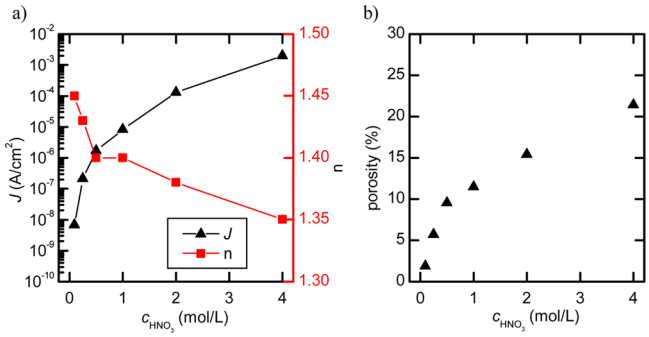

Figure 4. (a) Leakage current density at 1 MV/cm and refractive index for different SiO_x layers made from TEOS−sol solutions containing a HNO_3 concentration between 0.1 and 4 mol/L. (b) Derived porosity from the measured refractive index by the Lorentz−Lorenz relationship.

increasing molarities of nitric acid, while the refractive index decreases. The smaller refractive index indicates a higher porosity. A higher porosity leads to an increase of trap states within the dielectric layer. The trap states tend to enhance the Poole−Frenkel conduction mechanism,[22] which dominates the conduction at higher electric fields, as we will see later. The film porosity P was determined by the Lorentz−Lorenz equation:[32]

$$\frac{n^2 - 1}{n^2 + 2} = (1 - P)\frac{{n_0}^2 - 1}{{n_0}^2 + 2}$$

Here, n_0 is the refractive index of the dense SiO_2 (n_0 = 1.460).

The porosity of the film increases from 2% to 21% with an increasing amount of catalyst (Figure 4b). We assume that the higher concentration of nitric acid results in an accelerated gelation process and consequently in larger network structures. In these networks, liquids are encapsulated in small pores, which evaporate during the thermal treatment of the film. Thus, the porosity increases. It is important to control the gelation of the sol. In principle, the gelation of the sol can be influenced by the concentration of the catalyst or by the gelation time because a higher concentration of the catalyst leads to higher leakage current densities (Figure 4). The influence of the gelation time for a solution with the lowest possible concentration of the catalyst (c_{HNO_3} = 0.1 mol/L) was examined below. Figure 5 shows the current density with respect to the gelation time of a sol−gel solution containing nitric acid with a concentration of c_{HNO_3} = 0.1 mol/L. The findings indicate that the gelation time plays an important role in the sol−gel process. For solutions with gelation time of less than 3 h, it was not possible to form a silicon oxide film on the substrate. The first investigated silicon oxide layer with a gelation time of 3 h exhibits a leakage current density of about 1 μA/cm^2. The leakage current density decreases by 2 orders of magnitude for solutions, which gelatinize for 7 h. It was found that a gelation time of 6−7 h is

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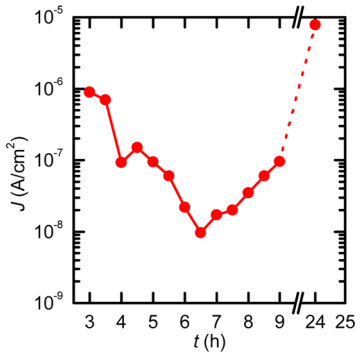

Figure 5. Leakage current density at 1 MV/cm for a SiO_x layer prepared from a solution with a TEOS precursor concentration of 0.8 mol/L and a HNO_3 concentration of 0.1 mol/L measured after different aging times (3−24 h). The red line has no physical meaning. It is only a guide for the eye.

the optimal time for this solution. After 7 h, the leakage current density increases with the aging time.

The decrease of the leakage current density within the first 7 h can be explained by the formation of siloxane (Si−O−Si) structures, which are necessary to form dense silicon oxide layers on the substrate. During the gelation, the network structure grows and small pores are created with water or alcohol containments. These liquids evaporate during the annealing process. In this way, current paths are formed in the dielectric layer, and they lead to an increase of the leakage current density. For the hydrolysis and condensation reaction, the structure of the gel is dependent on the time of gelation.[33] First of all, small particles are formed that are dispersed in the liquid, which is called a sol. These particles agglomerate to form a three-dimensional network of Si−O−Si bonds and is designated as a gel. We assume that the leakage current density increases when the gelation starts and the network structure begins to grow. Defects in the dielectric layer are created during the annealing process. If an electric field is applied, the charge carriers will move along the defect paths. With increasing electric field, additional defects are created and percolation paths are formed. Thus, the leakage current density increases.[34]

After optimization of the sol−gel solution and process parameters, it is necessary to investigate the suitability of the solution-processed silicon oxide as a gate dielectric. We compared the leakage current density and permittivity of the solution-processed SiO_x layer with a 230-nm-thick thermally grown SiO_2 layer. Figure 6a shows the leakage current density with respect to the applied electric field of the solution-processed silicon oxide compared to the thermally grown SiO_2. The solution contains nitric acid as the catalyst (c_{HNO_3} = 0.1 mol/L), has a TEOS concentration of c = 0.8 mol/L, and was aged for about 6.5 h. The resulting thickness of the oxide amounts to 143 nm. The current density in the solution-processed oxide at an electric field of 1 MV/cm is about 7×10^{-9} A/cm^2, which is similar to the thermally grown dielectric. At an applied field of 1.5 MV/cm, the current density of the solution-processed SiO_x starts to increase more over the applied electric field. We believe that the Poole−Frenkel conduction mechanism dominates for higher electric fields. The Poole−Frenkel mechanism can be mathematically described by

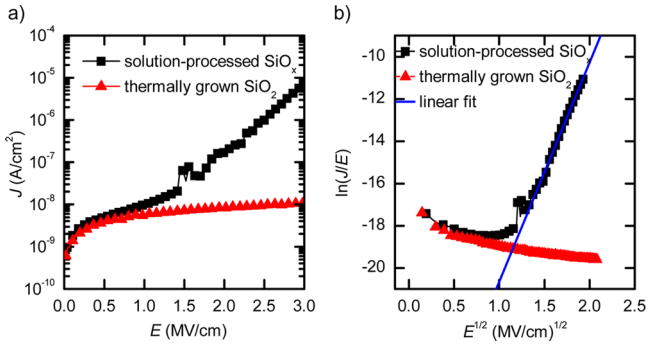

Figure 6. (a) Field-dependent leakage current density for a 143-nm-thick solution-processed SiO_x layer (black squares) and a 230 nm thermally grown SiO_2 layer (red triangles). (b) Poole−Frenkel plot for the solution-processed silicon oxide.

$$J_{PF} = qN_t\mu E \exp\left[-\frac{1}{kT}\left(q\phi_B - \sqrt{\frac{q^3E}{\pi\varepsilon_0\varepsilon_r}}\right)\right]$$

Here q, N_t, μ, $q\phi_B$, and ε_r denote the elementary charge, trap density, carrier mobility, barrier height of the traps, and dielectric constant of the oxide, respectively. Therefore, the Poole−Frenkel mechanism is dominant when the $\ln(J/E)$ versus $E^{1/2}$ is linear.[35] This is the case for the solution-processed SiO_x for $E^{1/2} > 1.0$ MV/cm but not for the thermally grown SiO_2 over the hole sweep range (Figure 6b). If the current flow is dominated by trap states, the barrier height between the trap states is lowered with increasing electric field. Thus, the charge carriers can move more easily from trap state to trap state. We conclude that the trap states are due to the higher porosity of the solution-processed dielectric compared to the thermally grown SiO_2. For a conversion temperature of T = 250 °C, the leakage current density increases by 2 orders of magnitude at E = 1 MV/cm (Figure S1 in the Supporting Information, SI). For applications on flexible substrates, the process must be further improved by using nonthermal conversion techniques, e.g., oxygen plasma treatment.[36]

The permittivity ε_r of the solution-processed SiO_x was calculated from $C-V$ measurements, which are shown in Figure 7. The measurements were performed at different frequencies ranging from 1 kHz to 1 MHz. Prior to any $C-V$ studies, the leakage current through the MIS devices was measured. In this

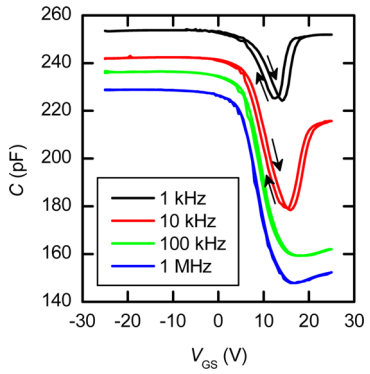

Figure 7. $C-V$ hysteresis of a solution-processed silicon oxide film at different frequencies (black, 1 kHz; red, 10 kHz; green, 100 kHz; blue, 1 MHz).

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regard, typical leakage currents were found to be on the order of 10^{-11} A.

For low frequencies (f = 1 and 10 kHz), the $C-V$ characteristics show clockwise hysteresis of about 2 and 1 V, respectively, which can be explained by the presence of trap states at the Si/SiO_x interface. At higher frequencies, the hysteresis disappears because the charge process of the trap states is too slow.[37] The permittivity is derived from the maximum capacitance in the accumulation regime, where the series capacitance of the depletion zone is negligible and the measured value corresponds to the oxide capacitance. The relationship between the capacitance and permittivity is given by the following equation:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

where C is the measured capacitance in the accumulation regime, $\varepsilon_0 = 8.854 \times 10^{-12}$ (A s)/(V m) is the permittivity of the vacuum, A is the contact area, and d is the thickness of the dielectric layer. The derived frequency-dependent permittivities for both the solution-processed and thermally grown SiO_2 are illustrated in Figure 8.

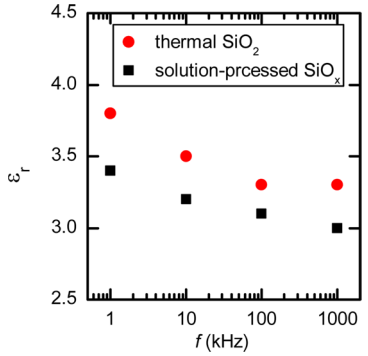

Figure 8. Derived frequency-dependent permittivities for the solution-processed SiO_x (black squares) and thermally grown SiO_2 (red circles).

The calculated permittivity of the solution-processed silicon oxide is in the range of the permittivity of the thermally grown oxide. We assume that the slightly lower permittivity results from residuals within the layer and from a higher porosity.

The low leakage current density and high electric breakdown field strength make the sol–gel-derived silicon oxide suitable for use as a gate dielectric in a TFT. Therefore, we used this dielectric combined with the solution-processed semiconductor iXsenic S in bottom-gate, bottom-contact TFTs (sample A) and compared the results with TFTs containing a thermally grown SiO_2 acting as a gate dielectric (sample B).

Typical output characteristics of transistors with a solution-processed and thermally grown SiO_x dielectric layer are displayed in Figure 9. Both transistors show similar characteristics. The TFT of sample A exhibits clear current saturation and pinch-off behavior, indicating that the entire thickness of the semiconductor channel layer can be depleted of free electrons. The transistor with thermally grown SiO_2 shows no clear saturation for higher gate voltages, which may result from the different oxide thicknesses.

Figure 10 displays the source–drain current I_{DS} and the mobility μ as a function of the electric field for typical TFTs of both samples. The transfer characteristics were measured at two

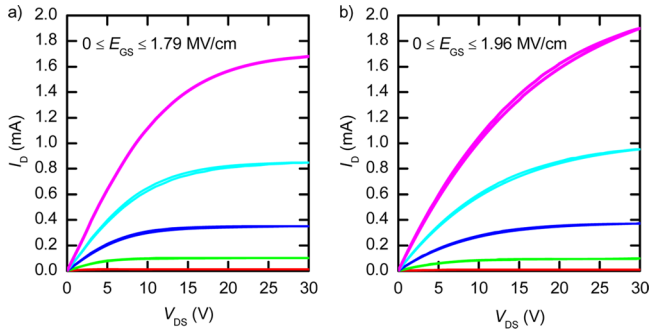

Figure 9. Output characteristics of bottom-contact transistors with (a) a 143-nm-thick solution-processed SiO_x gate dielectric and (b) a 230-nm-thick thermally grown SiO_2 gate dielectric.

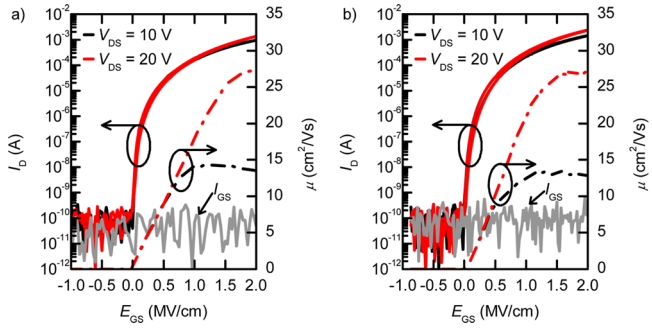

Figure 10. Transfer characteristics (solid line) and mobility versus the electric field E_{GS} (dash-dotted line) of a TFT with (a) a 143-nm-thick solution-processed insulator and (b) a 230 nm thermally grown SiO_2 layer. Furthermore, the leakage current I_{GS} through the dielectric layer is shown as a gray line.

different source–drain voltages, V_{DS1} = 10 V and V_{DS2} = 20 V. The gate voltage of sample A was swept between −20 and +30 V. Taking into account the higher thickness of the thermally grown SiO_2, the gate voltage for sample B was varied from −20 to +50 V. Hence, the electric field in sample B is comparable to the field generated in sample A. The solution-processed semiconductor iXsenic S works as an n-channel device, as can be seen from Figures 9 and 10. Both TFTs show a good on/off ratio of about 10^8, an onset voltage close to zero, and no hysteresis, indicating that no charge trapping in the bulk of the semiconductor or at the semiconductor/dielectric interface occurs. The mobility was calculated from the first derivative of the square root of the drain–source current:

$$\mu_{sat.} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2$$

Here, L and W denote the channel length and width of the transistors and C_i the gate dielectric capacitance per unit area. The derived mobility values are 14 $cm^2/(Vs)$ for V_{DS1} = 10 V and 28 $cm^2/(Vs)$ for V_{DS2} = 20 V. These values of the mobility are an upper limit because we used the dielectric constant for f = 1 kHz. The electrical parameters of the TFTs are comparable to recently achieved parameters based on solution-processed indium oxide TFTs.[38−46] (Further details given in Table S1 in the SI.)

The interface trap charge density N_s is directly related to the subthreshold swing S_{sub} by the following relationship:[47]

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$$N_s^{max} = \left(\frac{S_{sub} \log e}{kT/q} - 1 \right) \frac{C_i}{q}$$

Here, q is the electronic charge, k the Boltzmann constant, and T the absolute temperature. The subthreshold swing S_{sub} is extracted from the inverse of the maximum slope of the transfer characteristic. It indicates the gate voltage V_{GS}, which is required to increase I_{DS} by 1 decade.

$$S_{sub} = \left[\frac{d \log(I_{DS})}{dV_{GS}} \Big|_{max} \right]^{-1}$$

The subthreshold swing of the TFT from sample A (sample B) is around 0.30 V/dec (0.37 V/dec), which corresponds to a maximum interface trap density of 5.5×10^{11} cm^{-2} (5.9×10^{11} cm^{-2}). We believe the low interface trap density of the solution-processed silicon oxide is due to the smooth surface. The gate leakage current I_{GS} is also drawn in Figure 9 (gray lines). The leakage current of both devices is over the whole sweep range of V_{GS} below the noise level (100 pA) of the measurement equipment. The nearly identical electrical properties of the transistors underline the excellent quality of the solution-processed SiO_x, which is at least equivalent to thermally grown SiO_2.

CONCLUSIONS

We developed a high-quality solution-processed silicon oxide for TFT applications by a facile sol–gel reaction. We demonstrated the importance of the TEOS precursor concentration in the sol–gel solution to avoid film cracking and pinhole creation during the annealing process. The leakage current density and electric breakdown field strength were drastically improved by optimizing the catalyst content and gelation time. Optimal dielectric properties were achieved with a sol–gel solution containing nitric acid as the catalyst (c_{HNO_3} = 0.1 mol/L), a TEOS concentration of c = 0.8 mol/L, and a gelation time of 6.5 h. The applicability of the sol–gel solution was verified by metal oxide TFTs prepared with the solution-processed SiO_x and a solution-processed indium-based metal oxide. They exhibit a field-effect mobility of 28 cm^2/(Vs), an on/off ratio of 10^8, no hysteresis, an onset voltage close to zero, and a small interface trap density (5.9×10^{11} cm^{-2}). The obtained electrical properties of the TFTs with solution-processed silicon oxide are at least equivalent to those with thermally grown SiO_2. Because thermally grown SiO_2 requires a silicon substrate, the solution-processed silicon oxide has a decisive advantage. It can be used on many other substrates, e.g., glass or compound semiconductors. The first results were achieved on a glass substrate (Figure S2 in the SI).

ASSOCIATED CONTENT

Supporting Information

Leakage current density for the solution-processed silicon oxide at a maximum temperature of 250 °C, recently published mobility values for solution-processed indium oxide based TFTs, and leakage current density for the solution-processed silicon oxide coated on glass/ITO substrates. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.5b03105.

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Notes

The authors declare no competing financial interest.

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